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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,279	12/21/2000	Martin Czech	Micronas.5923	9347

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EXAMINER	
LEFKOWITZ, SUMATI	

ART UNIT	PAPER NUMBER
2112	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/747,279	Applicant(s) CZECH ET AL.	
	Examiner Sumati Lefkowitz	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are pending.

Drawings

2. The drawings are objected to because

- Figures 1 and 2 should be labeled "PRIOR ART"
- In Figure 1, elements 1, 2, and 3 should be labeled with textual descriptions
- In Figure 2, elements 3, 14, 13-15 should be labeled with textual descriptions
- In Figure 2, both the data bus 14 and one of the receivers 14 have the same element number
- In Figure 3, elements 30, 32, and 48 should be labeled with textual descriptions
- In Figure 4, elements 54 and 56 should be labeled with textual descriptions

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Using Inherent Capacitance of a Bus To Perform Data Storage During Data Transfer Across the Bus".

4. The abstract of the disclosure is objected to because

- it fails to disclose that the data bus takes over the role of the master memory device via its inherent capacitance

Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claim 5 is/are objected to because of the following informalities:

As to claim 5, it seems that claim 5 should depend from claim 1, not claim 2, as claim 2 recites that the first memory element is an inherent parasitic capacitance associated with the bus and claim 5 recites that the first memory element is a holding element. The specification, however, discloses that the inherent parasitic capacitance and holding element are alternatives for the first memory element, not complements to each other, so claim 5 should not depend from claim 2. Please note that the claim 5 will be rejected on this basis, i.e., as it depends from claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1, 5, 9, and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (hereinafter AAPA).

a. As to claims 1, 5, and 9, AAPA discloses a circuit arrangement for transferring data between a data transmitter (note Figure 2, element 10) and a data receiver (note Figure 2, element 12), said circuit arrangement comprising: a buffer device (note Figure 2, element 16) that receives a data signal from the data transmitter and provides a buffered data signal onto a data bus (note Figure 2, element 14); a first memory element (note Figure 2, element 20) that receives and stores said buffered signal on said data bus and provides a first stored signal; a second memory element (note Figure 2, element 22) that receives and stores said first stored signal and provides a second stored signal to the data receiver; and a controller (note Figure 2, element 24) that controls the output state of said buffer device, to control the transfer of data from said first memory element to said second memory element (note Figure 2 and page 1, [0005]). AAPA also discloses that the first memory device comprises a dedicated memory element that comprises a holding element (note Figure 2, first memory device 20). AAPA also discloses that the circuit arrangement has at least one microprocessor/microcontroller and/or at least one signal processor with a given set of states (note page 1, [0004-0005]).

b. As to claim 11, AAPA discloses an integrated circuit arrangement for transferring data between a data transmitter (note Figure 2, element 10) and a data receiver (note Figure 2, element 12), said circuit arrangement comprising: means for receiving (note Figure 2, element 16) a data signal from the data transmitter and for providing a buffered data signal onto a data bus (note Figure 2, element 14); a first memory element (note Figure 2, element 20) that receives and stores said buffered signal on said data bus, and provides a first stored signal; a second

memory element (note Figure 2, element 22) that receives and stores said first stored signal, and provides a second stored signal to the data receiver; and a controller (note Figure 2, element 24) that controls the output state of said means for receiving, such that when said means for receiving provides a high impedance output data is transferred from said first memory element to said second memory element (note Figure 2 and page 1, [0005]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 2, 3, 4, 6, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of Wyatt et al., 4,567,561 (hereinafter Wyatt).

a. As to claims 2, 3, 4, and 10, AAPA fails to disclose that the first memory element is comprised of an inherent parasitic capacitance associated with said data bus, or that the first memory device is constructed as a capacitive element, one of whose terminals is connected to said data bus, and whose other terminal is connected to a reference potential, or that the capacitance of the capacitive element is provided by the line capacitance of said data bus with respect to one or more reference lines, or that the first memory element consists of parasitic capacitance associated with said data bus.

Wyatt discloses a memory element comprised of an inherent parasitic capacitance associated with a data bus, that a memory device is constructed as a capacitive element, one of whose terminals is connected to said data bus, and whose other terminal is connected to a reference potential, and that the capacitance of the capacitive element is provided by the line capacitance of said data bus with respect to one or more reference lines, and that the first memory element consists of parasitic capacitance associated with said data bus (note abstract, column 1, line 40 – column 2, line 3, column 11, line 46 – column 12, line 33).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of the inherent parasitic capacitance associated with a bus to store data on the bus in place of a discrete memory element, as Wyatt teaches, in the system of AAPA so as to reduce hardware requirements, and associated costs, as well as increase the performance speed in that no additional steps are required to move the data into or out of a separate buffer register.

b. As to claim 6, AAPA discloses that the controller controls said data buffers associated with the data transmitter and the data receivers and the second memory devices.

10. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of what was asserted to be well known in the art, as exemplified by Moore et al., 6,378,011 (hereinafter Moore) and Shimizu, 5,293,378.

a. As to claim 7, AAPA fails to disclose that the controller comprises: a first control section, associated with the data transmitter, for controlling the first data buffer; and a second control section, associated with each of the data receivers, that controls second data buffers and said second memory devices, a control data communication between the data transmitter and the data receiver.

Examiner takes Official Notice that having separate controllers, one associated with a transmitter and another associated with a receiver is well known in the art of signal transmission for providing independent control of data transmission and reception, as evidenced by Moore et al. -- 6,378,011 (note Figure 1, ASD TX Control 107 and ASD RX Control 108) and Shimizu -- 5,293,378 (note Figure 1, transmission controller 10 and reception controller 20).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of separate TX and RX controllers, as Moore et al. and Shimizu teach, in the system of AAPA so as to provide independent, and therefore more flexible control, over the transmission and reception of data across the bus.

b. As to claim 7, AAPA discloses that at least one of the circuit sections is part of a peripheral region of the integrated circuit for accepting the connection pads of the input/output connections (note Figure 1 and page 1, [0002-0003]).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the prior art teaches or suggests taking advantage of the inherent capacitance of a bus during data transfer.

US Patents:	5,028,810	Castro et al.	4,961,002	Tam et al.
	4,956,564	Holler et al.	4,537,471	Grinberg et al.
	4,829,515	Donaldson et al.	4,774,422	Donaldson et al.
	4,500,988	Bennett et al.		

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790. The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-4815.

The fax phone numbers for the organization where this application or proceeding is assigned are:

703-746-7238	for After-Final communications
703-872-9306	for Official communications
703-746-5661	for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Sumati Lefkowitz
Primary Examiner
Art Unit 2112

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February 10, 2004